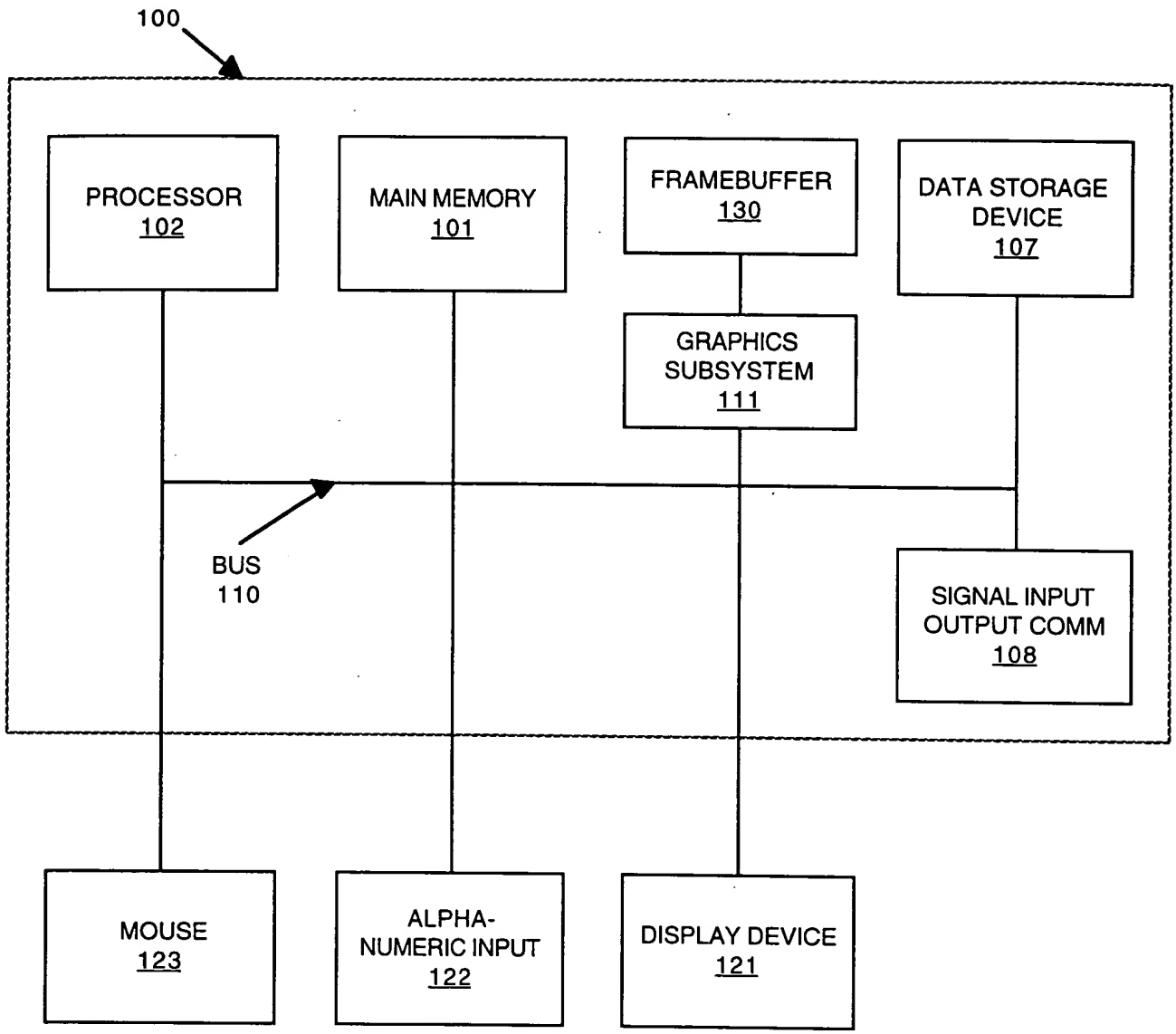

100
PROCESSOR
102
MAIN MEMORY
101
FRAMEBUFFER
130
DATA STORAGE
DEVICE
107
GRAPHICS
SUBSYSTEM
111
BUS
110
SIGNAL INPUT
OUTPUT COMM
108
MOUSE
123
ALPHA-
NUMERIC INPUT
122
DISPLAY DEVICE
121

Figure 1

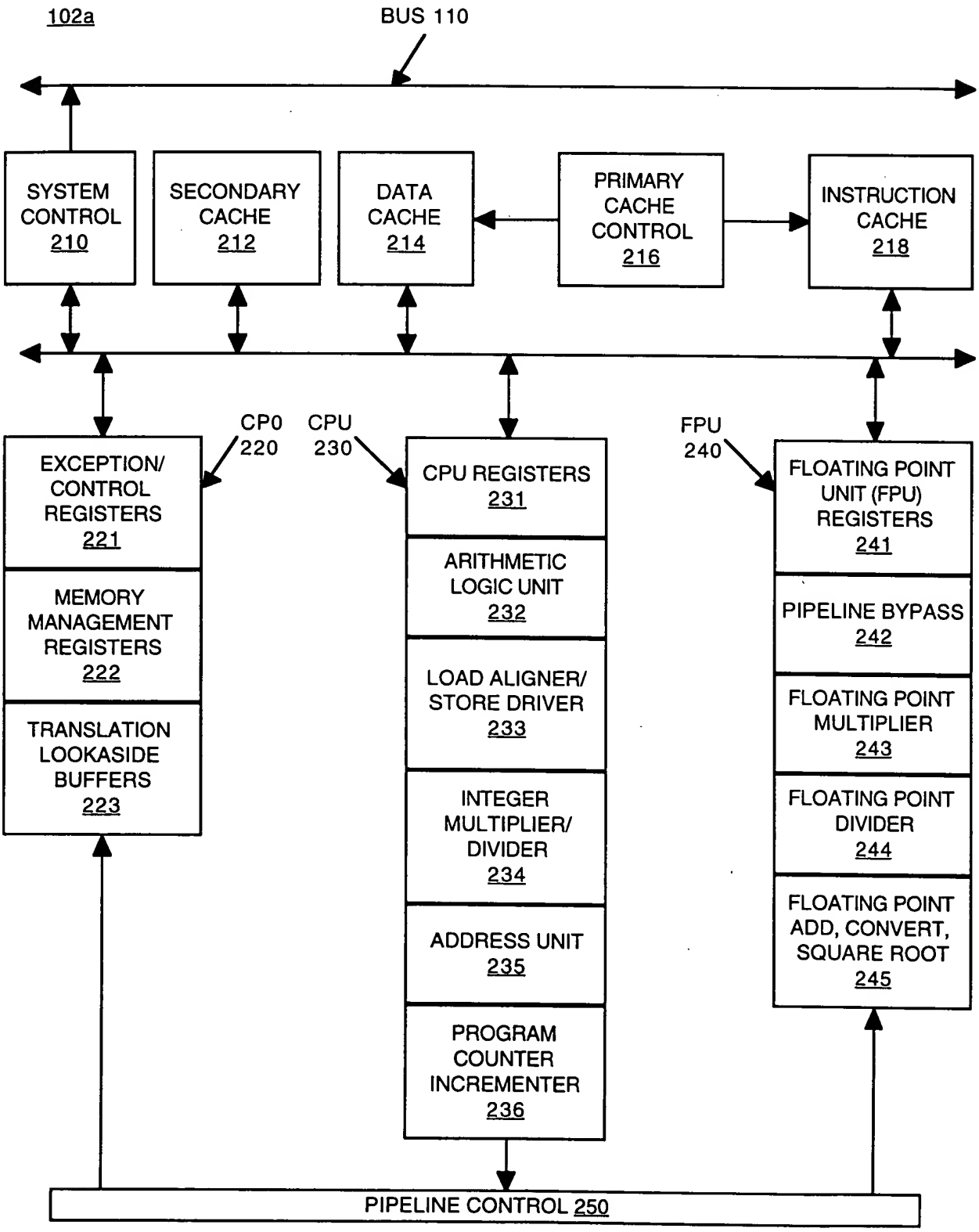

102a
BUS 110
SYSTEM CONTROL 210
SECONDARY CACHE 212
DATA CACHE 214
PRIMARY CACHE CONTROL 216
INSTRUCTION CACHE 218
CP0 220
CPU 230
FPU 240
EXCEPTION/ CONTROL REGISTERS 221
MEMORY MANAGEMENT REGISTERS 222
TRANSLATION LOOKASIDE BUFFERS 223
CPU REGISTERS 231
ARITHMETIC LOGIC UNIT 232
LOAD ALIGNER/ STORE DRIVER 233
INTEGER MULTIPLIER/ DIVIDER 234
ADDRESS UNIT 235
PROGRAM COUNTER INCREMENTER 236
FLOATING POINT UNIT (FPU) REGISTERS 241
PIPELINE BYPASS 242
FLOATING POINT MULTIPLIER 243
FLOATING POINT DIVIDER 244
FLOATING POINT ADD, CONVERT, SQUARE ROOT 245
PIPELINE CONTROL 250

Figure 2A

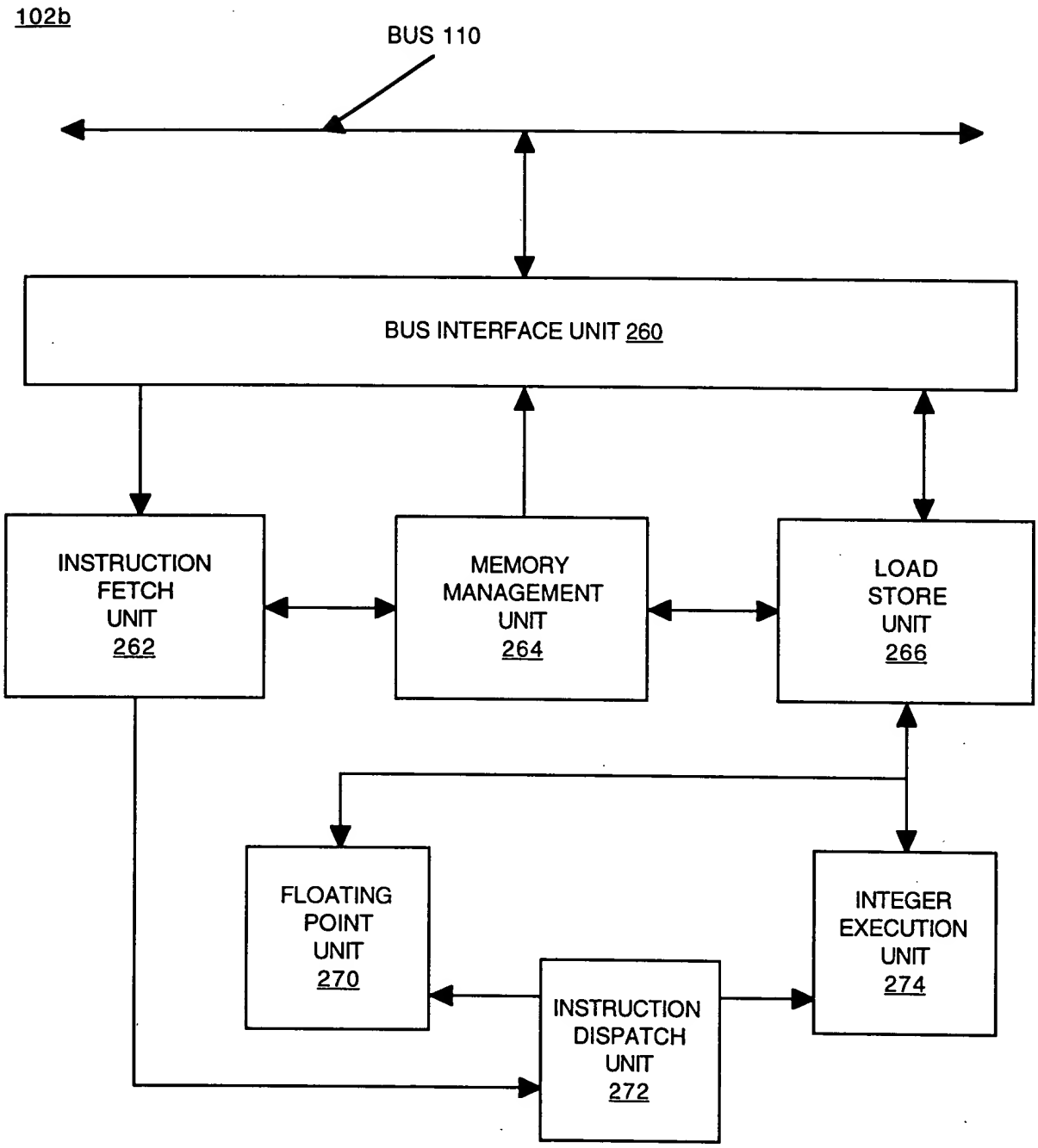

102b
BUS 110
BUS INTERFACE UNIT 260
INSTRUCTION FETCH UNIT 262
MEMORY MANAGEMENT UNIT 264
LOAD STORE UNIT 266
FLOATING POINT UNIT 270
INSTRUCTION DISPATCH UNIT 272
INTEGER EXECUTION UNIT 274

Figure 2B

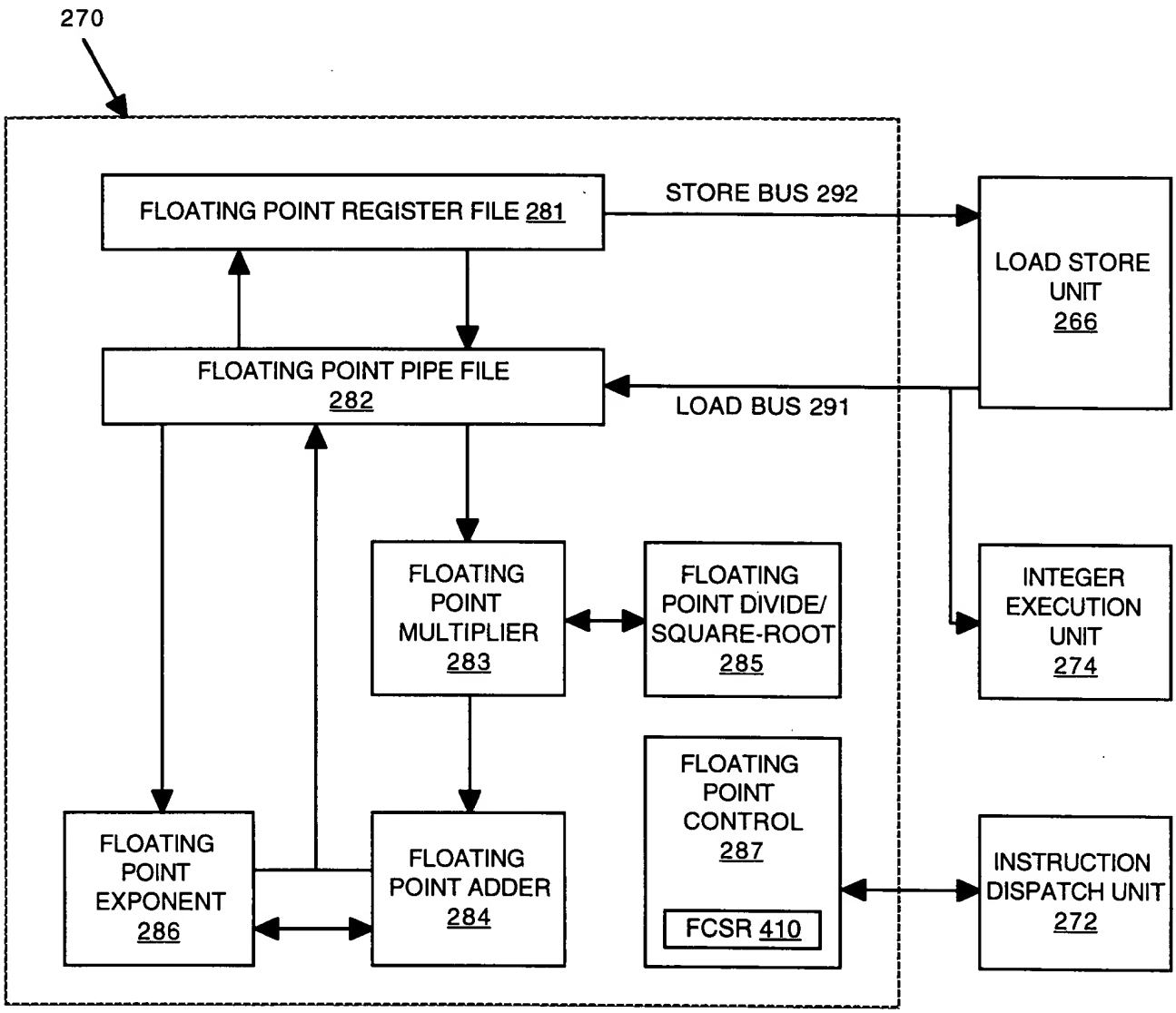

270
FLOATING POINT REGISTER FILE 281
STORE BUS 292
LOAD STORE UNIT 266
FLOATING POINT PIPE FILE 282
LOAD BUS 291
FLOATING POINT MULTIPLIER 283
FLOATING POINT DIVIDE/ SQUARE-ROOT 285
INTEGER EXECUTION UNIT 274
FLOATING POINT EXPONENT 286
FLOATING POINT ADDER 284
FLOATING POINT CONTROL 287
FCSR 410
INSTRUCTION DISPATCH UNIT 272

Figure 2C

270

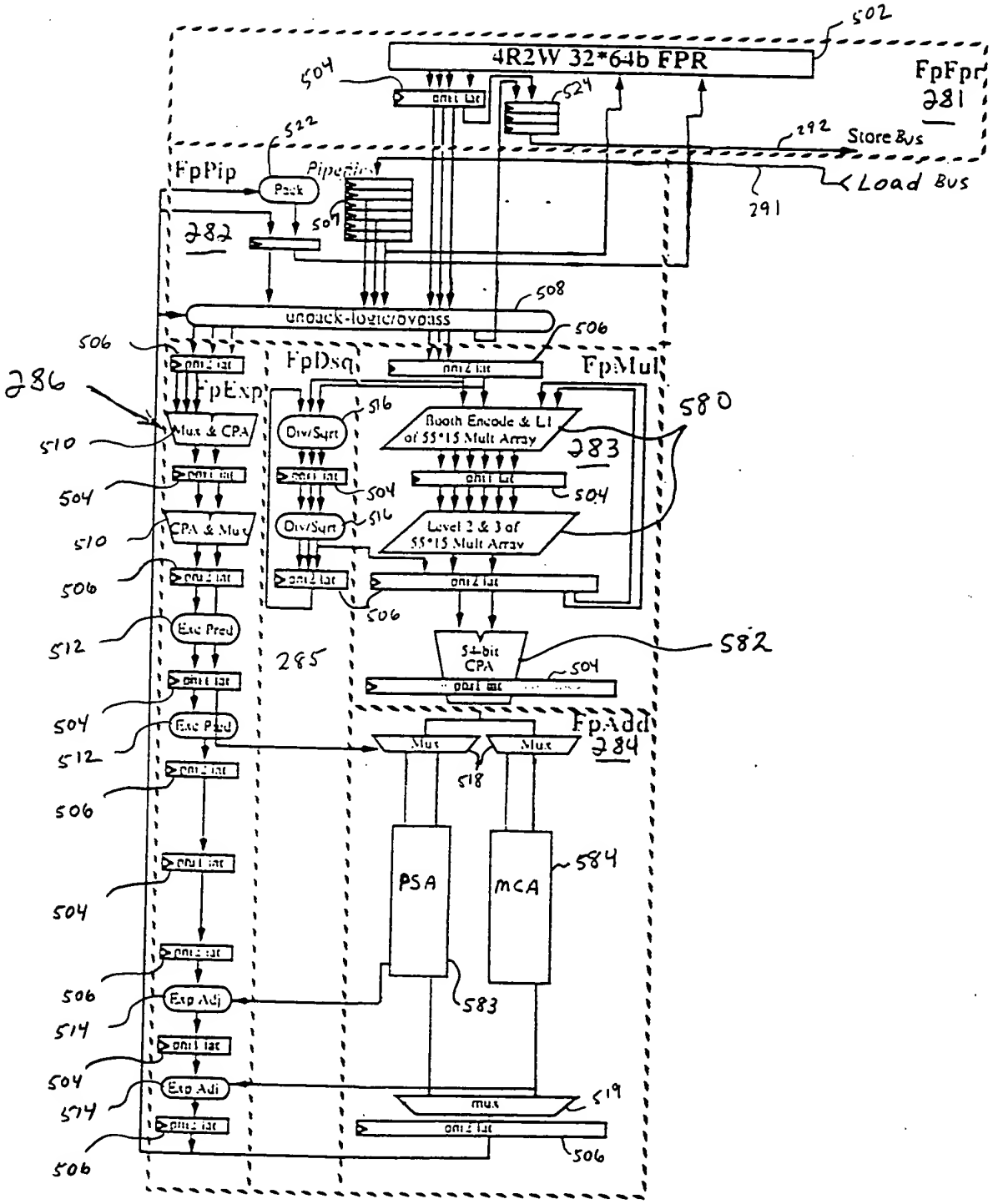


Figure 2D

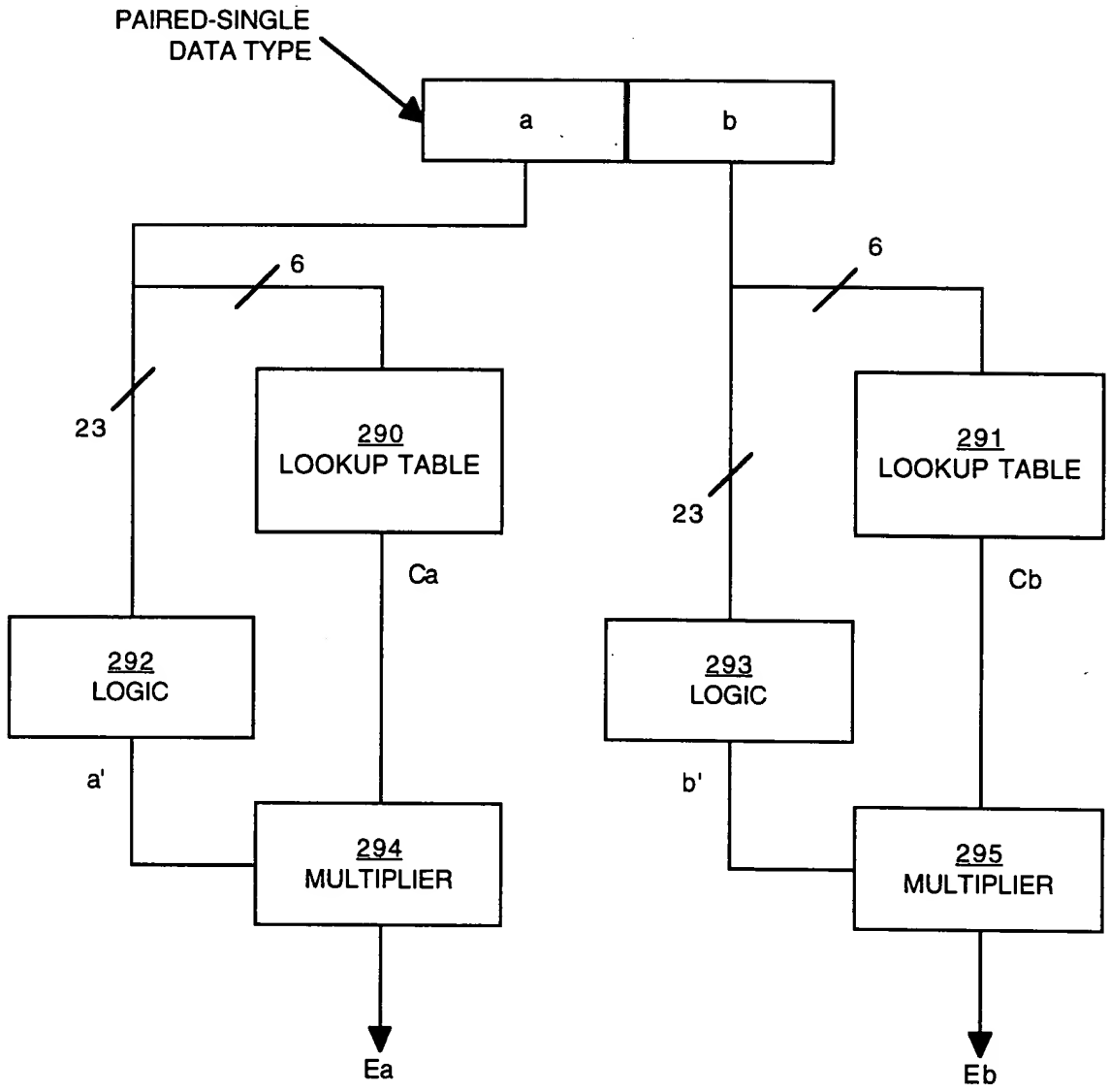

PAIRED-SINGLE
DATA TYPE
a
b
6
6
23
23
290
LOOKUP TABLE
291
LOOKUP TABLE
Ca
Cb
292
LOGIC
293
LOGIC
a'
b'
294
MULTIPLIER
295
MULTIPLIER
Ea
Eb

Figure 2E

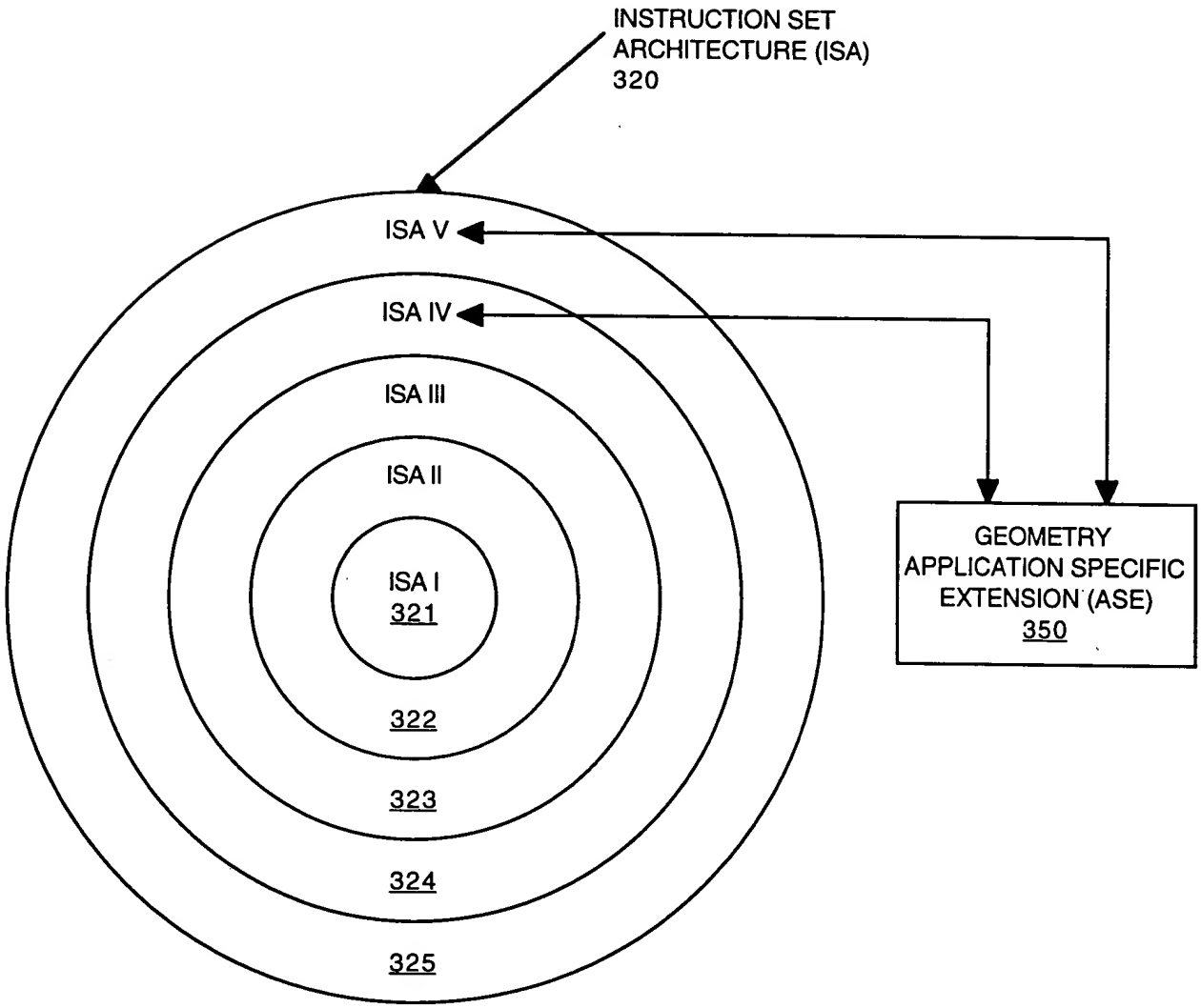

INSTRUCTION SET
ARCHITECTURE (ISA)
320
ISA V
ISA IV
ISA III
ISA II
ISA I
321
322
323
324
325
GEOMETRY
APPLICATION SPECIFIC
EXTENSION (ASE)
350

Figure 3

6606Z0" 98Z49E60

410

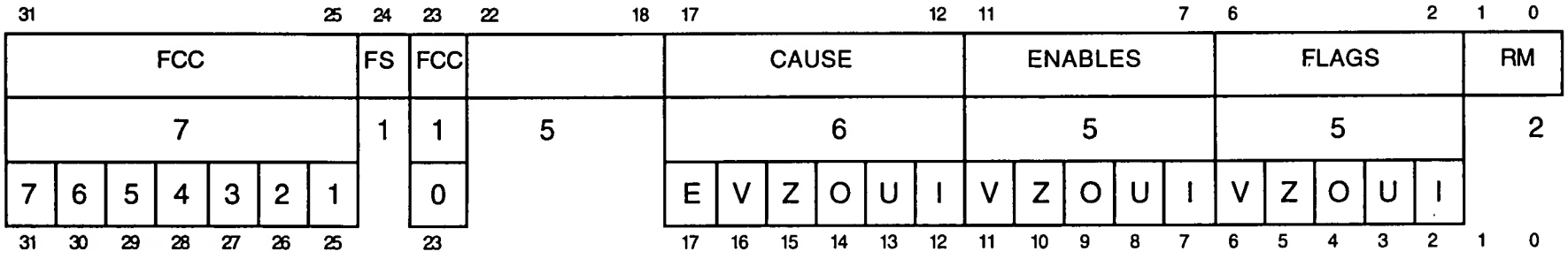


Figure 4

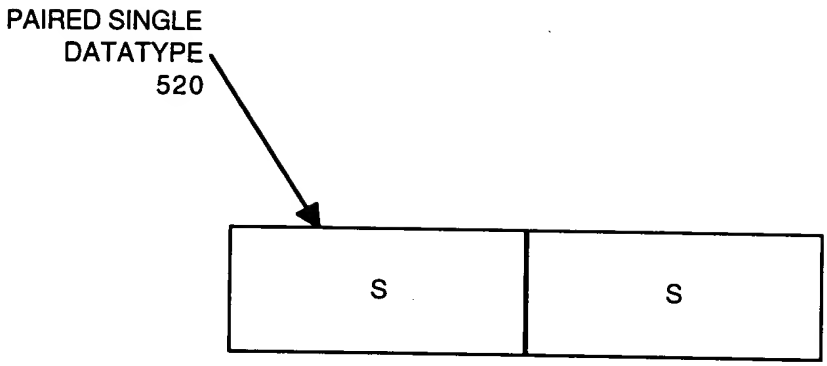
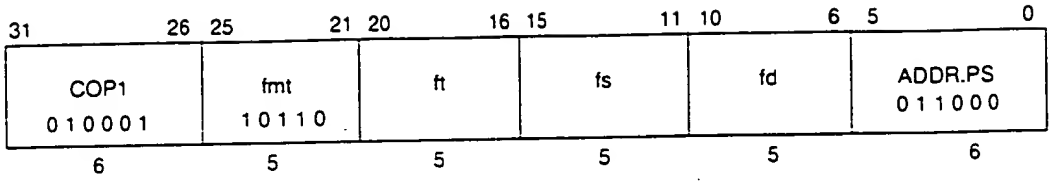


Figure 5

0 0 0

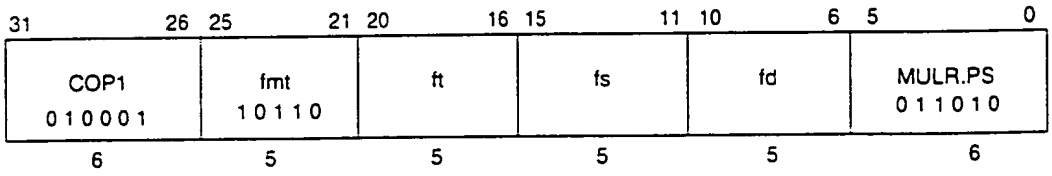
ADDR 601



Format: ADDR.PS fd, fs, ft

Figure 6A

MULR 602

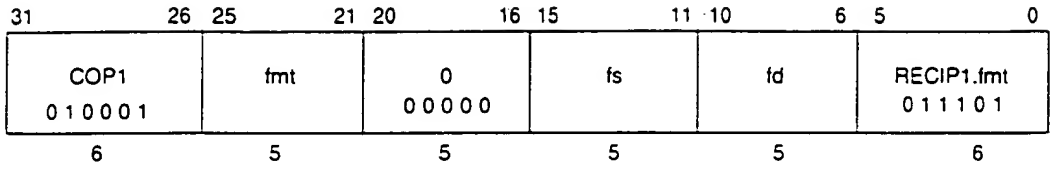


Format: MULR.PS fd, fs, ft

Figure 6B

Document ID: US 6,675,285 B1

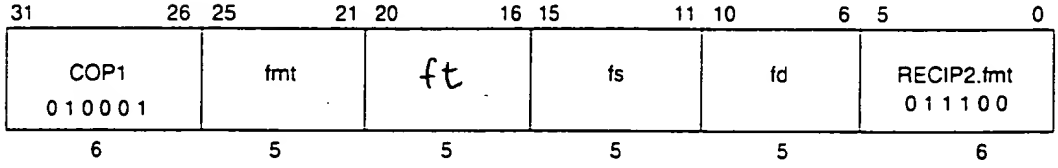
RECIP1 603



Format: RECIP1.S fd, fs
RECIP1.D fd, fs
RECIP1.PS fd, fs

Figure 6C

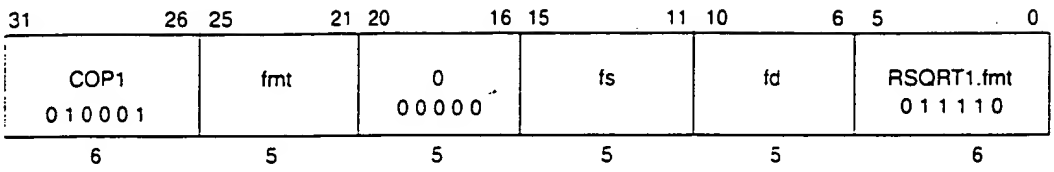
RECIP2 604



Format: RECIP2.S fd, fs, ft
RECIP2.D fd, fs, ft
RECIP2.PS fd, fs, ft

Figure 6D

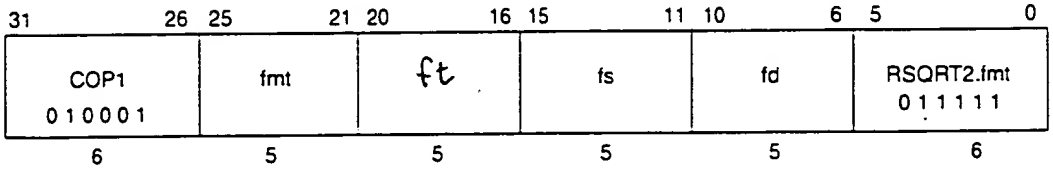
RSQRT1 605



Format: RSQRT1.S fd, fs
RSQRT1.D fd, fs
RSQRT1.PS fd, fs

Figure 6E

RSQRT2 606

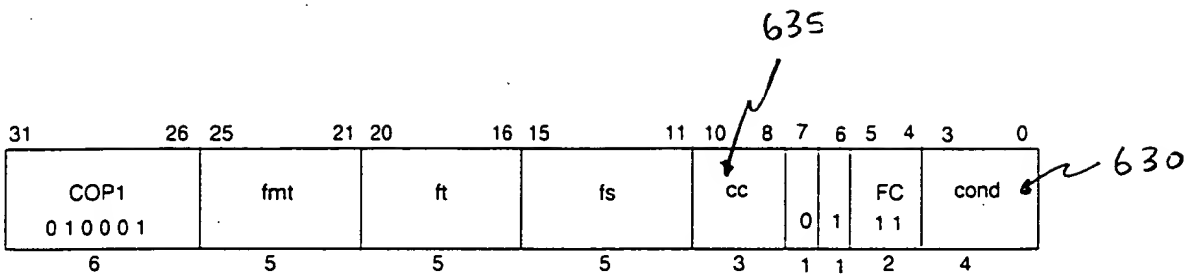


Format: RSQRT2.S fd, fs, ft
RSQRT2.D fd, fs, ft
RSQRT2.PS fd, fs, ft

Figure 6F

0050-0050-0050

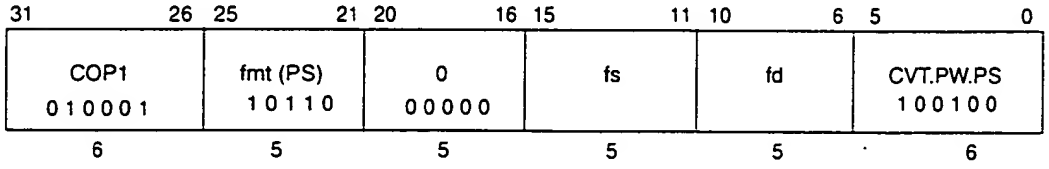
CABS 607



Format: CABS.cond.S cc, fs, ft
CABS.cond.D cc, fs, ft
CABS.cond.PS cc, fs, ft

Figure 6G

CVT.PW.PS 608



Format: CVT.PW.PS fd, fs

Figure 6H

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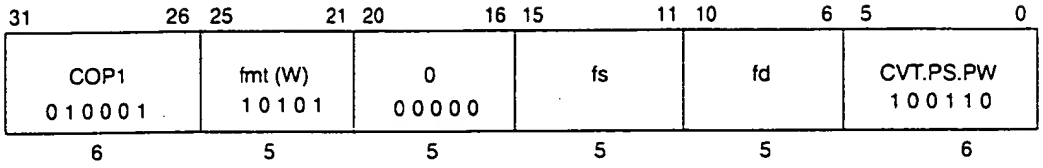
CVT.PS.PW 609

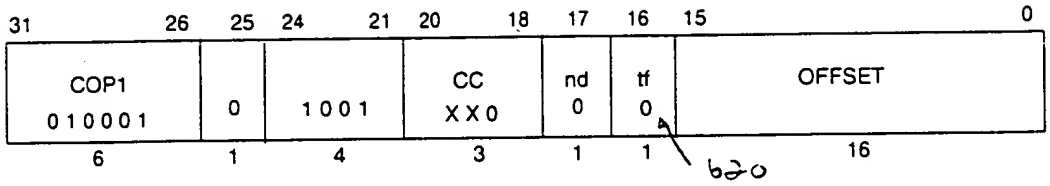


Format: CVT.PS.PW fd, fs

Figure 6I

Google Exhibit 1005 - Page 0609

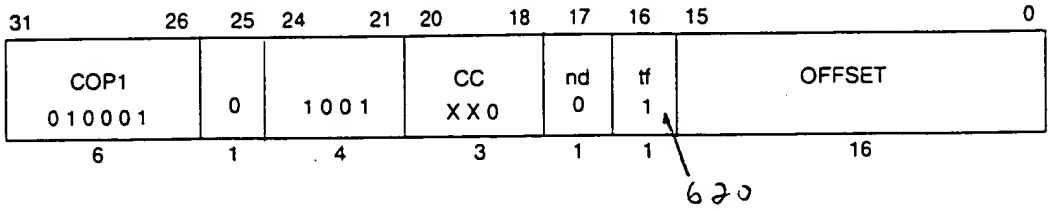
BC1ANY2F 610



Format: BC1ANY2F cc, offset

Figure 6J

BC1ANY2T 611

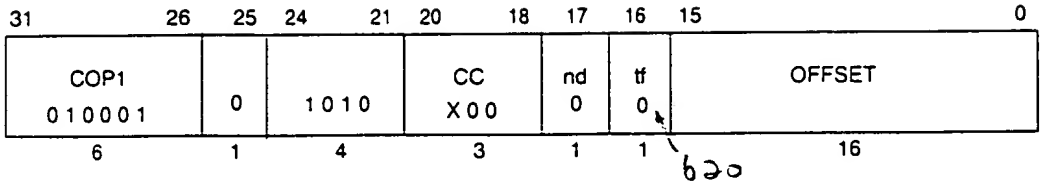


Format: BC1ANY2T cc, offset

Figure 6K

Document ID: 0500-0005-0000

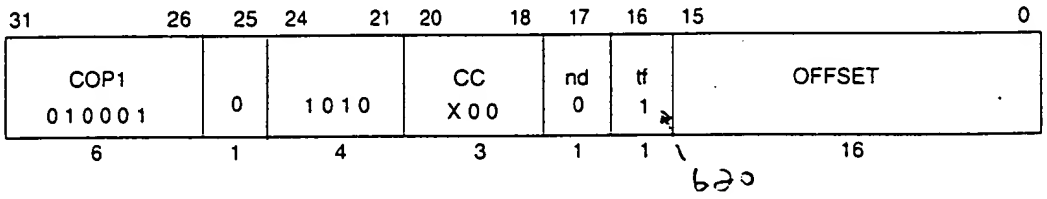
BC1ANY4F 612



Format: BC1ANY4F cc, offset

Figure 6L

BC1ANY4T 613



Format: BC1ANY4T cc, offset

Figure 6M

0 6 0 5 4 9 6 5 - 0 0 0 0 5

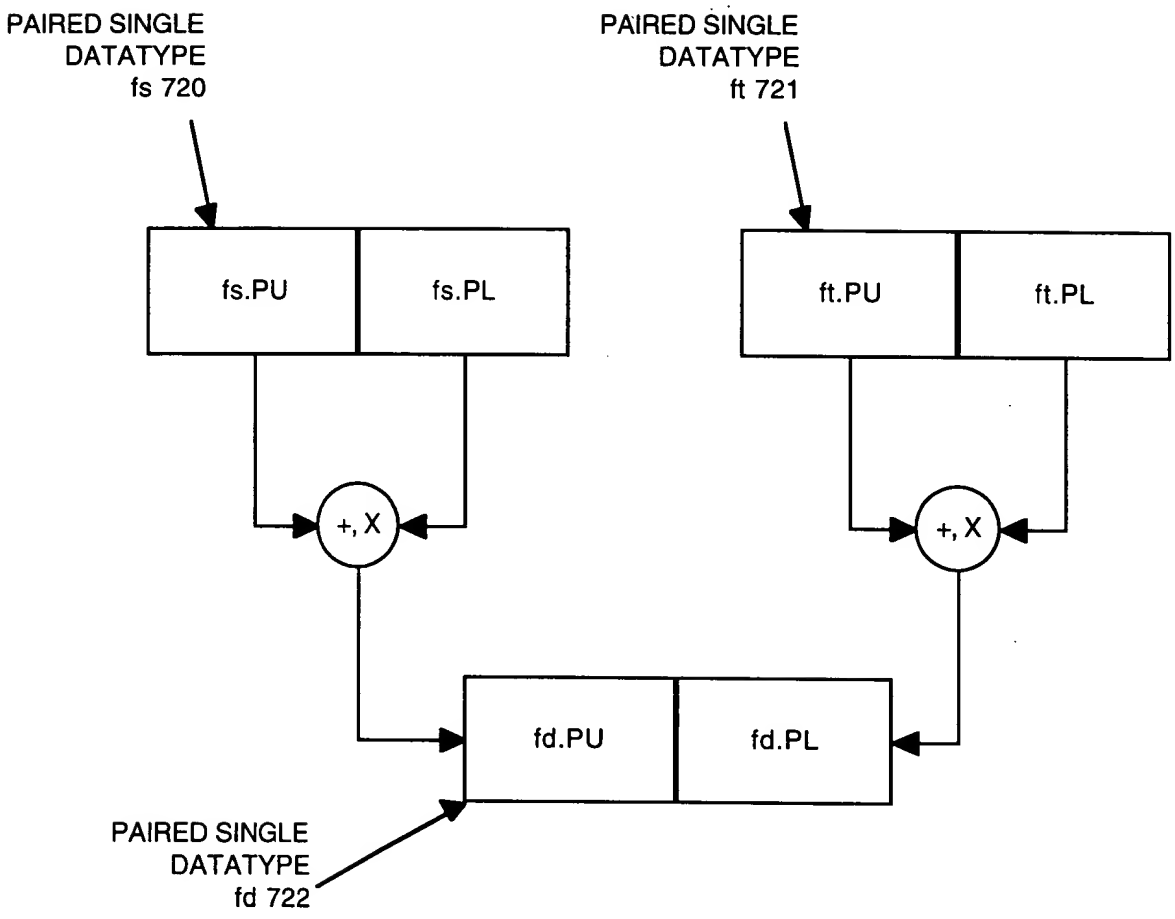

PAIRED SINGLE
DATATYPE
fs 720
PAIRED SINGLE
DATATYPE
ft 721
fs.PU
fs.PL
ft.PU
ft.PL
+, X
+, X
fd.PU
fd.PL
PAIRED SINGLE
DATATYPE
fd 722

Figure 7A

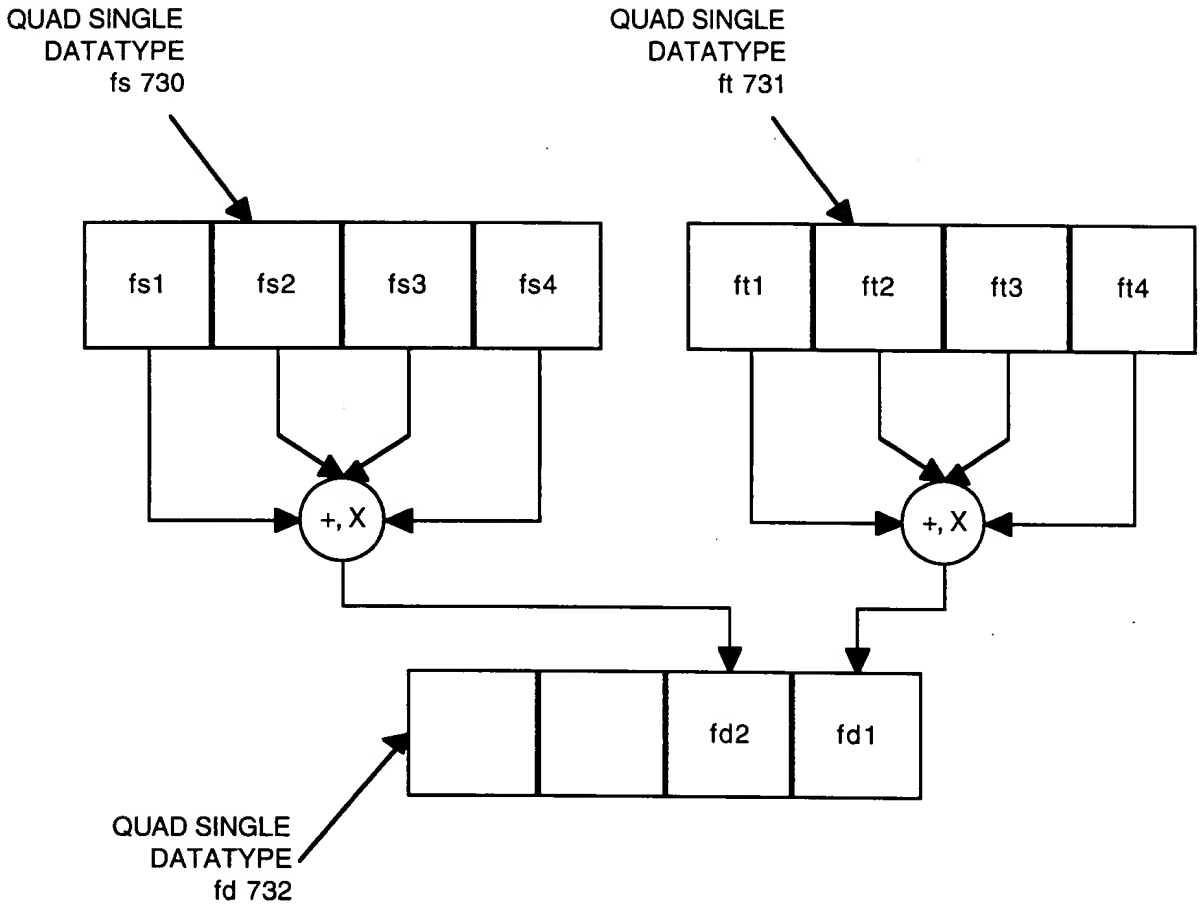
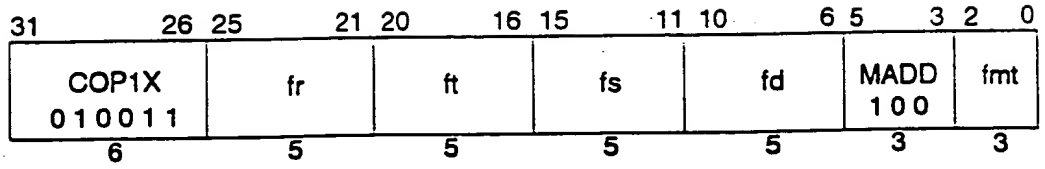

QUAD SINGLE
DATATYPE
fs 730
QUAD SINGLE
DATATYPE
ft 731
fs1
fs2
fs3
fs4
ft1
ft2
ft3
ft4
+, X
+, X
fd2
fd1
QUAD SINGLE
DATATYPE
fd 732

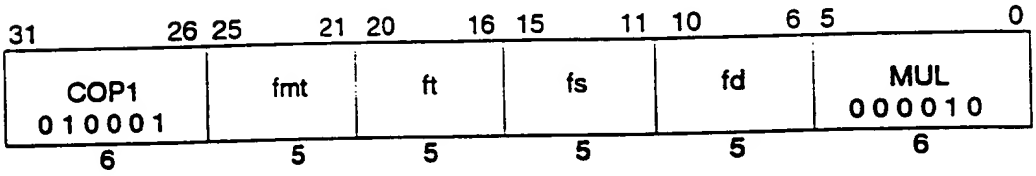
Figure 7B

MADD 801



Format: MADD.S fd, fr, fs, ft
MADD.D fd, fr, fs, ft
MADD.PS fd, fr, fs, ft

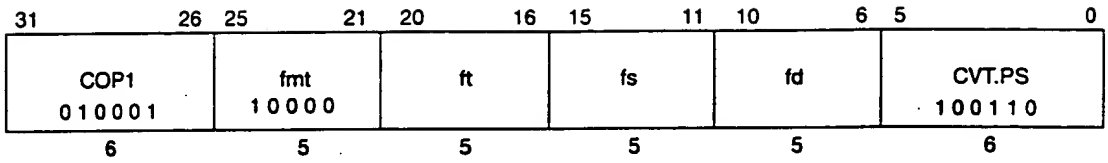
Figure 8



Format: MUL.S fd, fs, ft
MUL.D fd, fs, ft
MUL.PS fd, fs, ft

Figure 9

CVT.PS.S 1001



Format: CVT.PS.S fd, fs, ft

Figure 10

0 6 0 5 4 9 8 6 - 0 0 0 0 6

1000

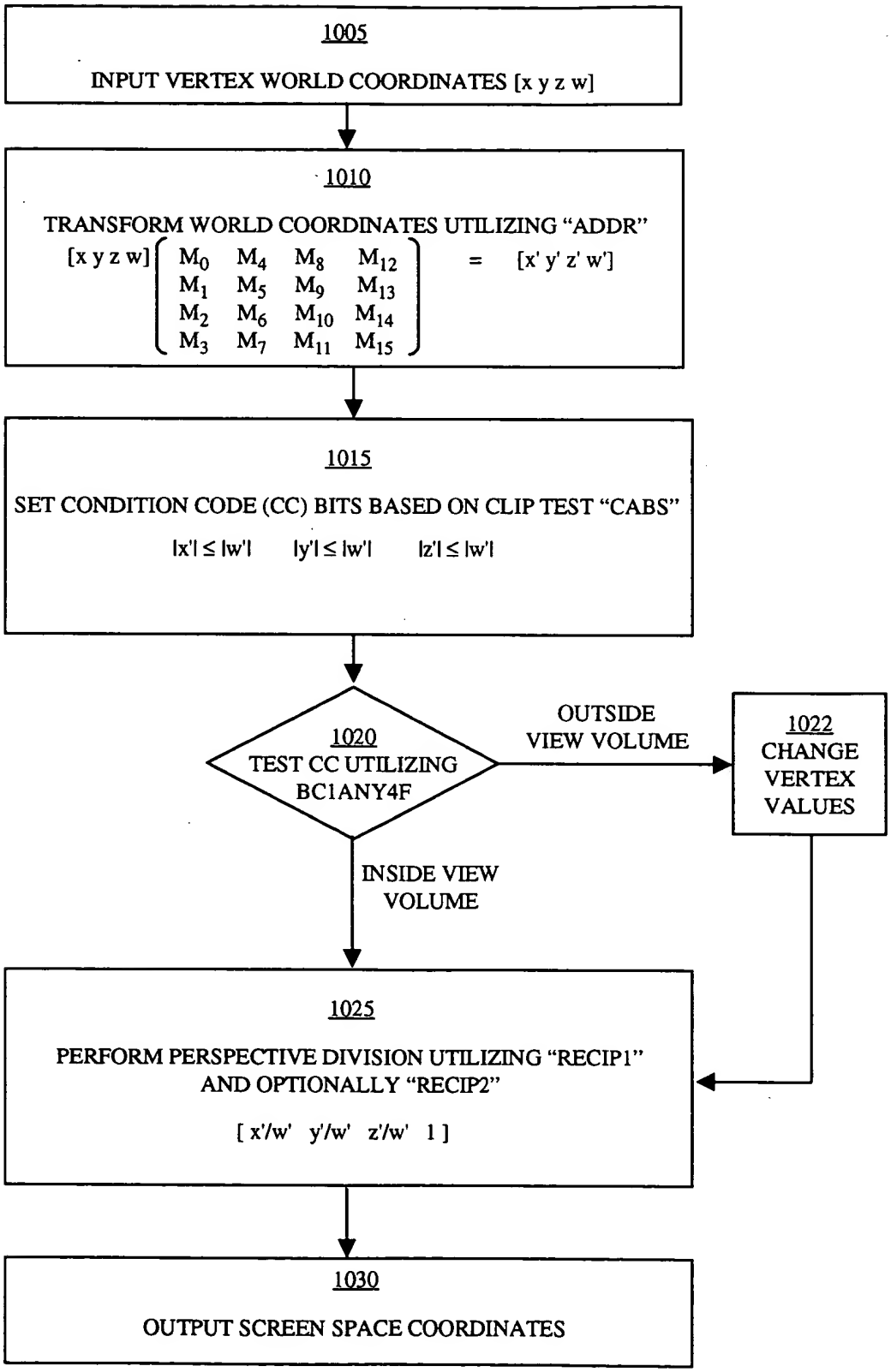


Figure 11A

1100

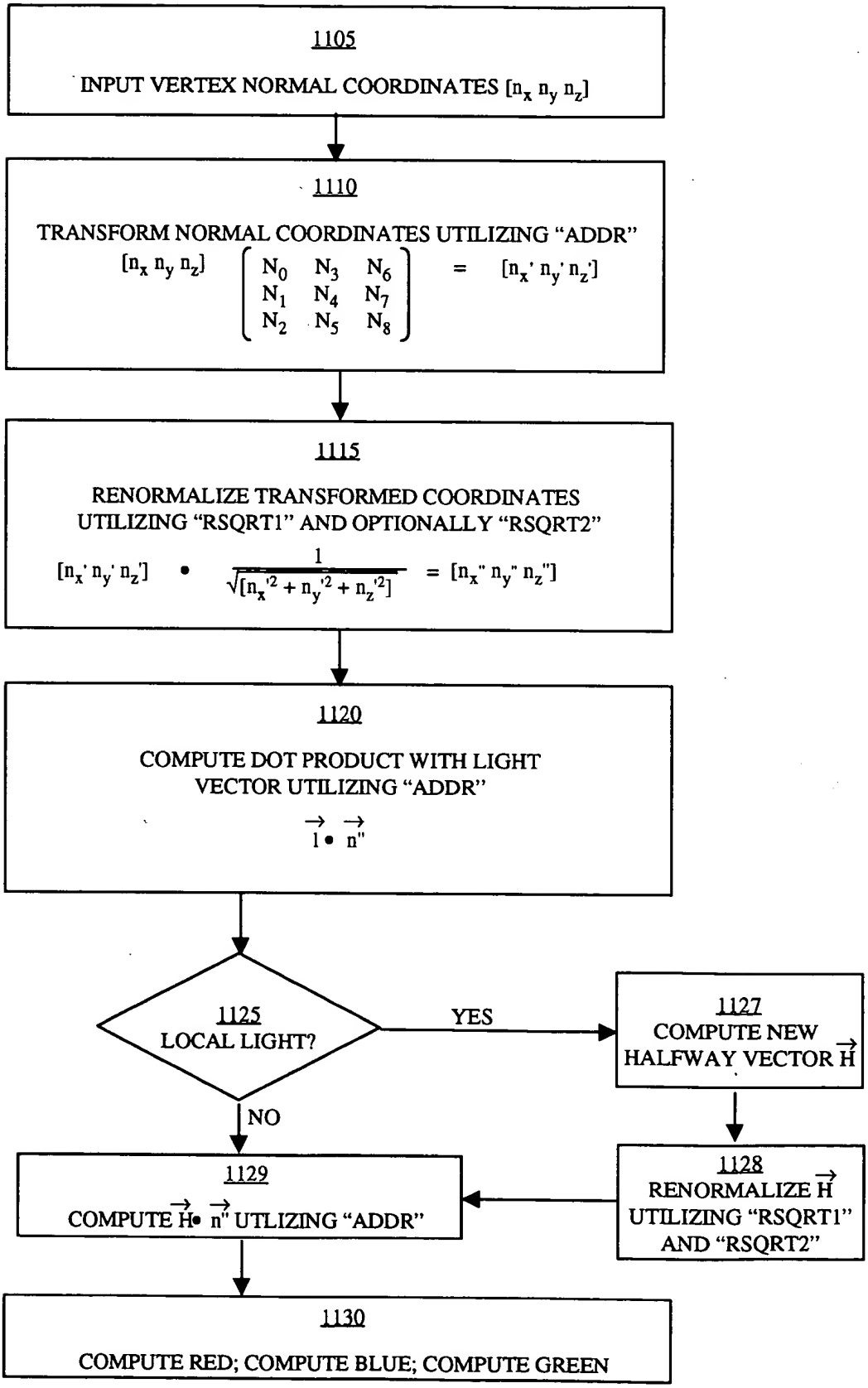


Figure 11B

660620 9824960

3D Matrix Transform

[x, y, z, w] * $\begin{bmatrix} M_0 & M_4 & M_8 & M_{12} \\ M_1 & M_5 & M_9 & M_{13} \\ M_2 & M_6 & M_{10} & M_{14} \\ M_3 & M_7 & M_{11} & M_{15} \end{bmatrix}$

```
# fp0-fp7 contain the 4x4 matrix in pair single format
# base contains the address of the next vector as two pair single values
      ld        fp10, 0(base)          # fp10: y || x
      ld        fp11, 8(base)          # fp11: w || z
# fp10 available here assuming L1 cache hit.  Use prefetch to accomplish this
      mul.ps fp14, fp10, fp4           # fp14: M9y || M8x
      mul.ps fp15, fp10, fp6           # fp15: M13y || M12x
      mul.ps fp12, fp10, fp0           # fp12: M1y || M0x
      mul.ps fp13, fp10, fp2           # fp13: M5y || M4x

# fp14 available here
      madd.ps fp14, fp14, fp11, fp5    # fp14: M11w+M9y || M10z+M8x
      madd.ps fp15, fp15, fp11, fp7    # fp15: M15w+M13y || M14z+M12x
      madd.ps fp12, fp12, fp11, fp1    # fp12: M3w+M1y || M2z+M0x
      madd.ps fp13, fp13, fp11, fp3    # fp13: M7w+M5y || M6z+M4x

      ssnop
# fp14, fp15 available here
      addr.ps fp11, fp15, fp14         # fp11: w' || z'
                                       # fp11: M15w+M14z+M13y+M12x || M11w+M10z+M9y+M8x

# fp12, fp13 available here
      addr.ps fp10, fp13, fp12         # fp10: y' || x'
                                       # fp10: M7w+M6z+M5y+M4x || M3w+M2z+M1y+M0x
```

FIG. 12